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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,158	09/26/2001	Martin Li	TI-33430	9577

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EXAMINER	
GREY, CHRISTOPHER P	
ART UNIT	PAPER NUMBER
2667	

DATE MAILED: 05/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,158	LI, MARTIN	
	Examiner	Art Unit	
	Christopher P Grey	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

The examiner would greatly appreciate that the corresponding application numbers to the given related applications be provided (Page 1 lines 11-24).

Appropriate correction is required.

Claim Objections

2. Claims 1 and 5 are objected to because of the following informalities:

(a) Regarding claim 1, it is unclear to the examiner what is being claimed on page 11, lines 13-15. The manner in which the sentence is worded/constructed is unclear.

(b) Regarding claim 5, there are grammatical errors in the following, "the destination locations can selected". Furthermore, the claim is unclear to the examiner.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 7, 8, 14 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Jensen et al. (6732206).

Claim 1 Jensen et al. ('Jensen' hereinafter) discloses an ATM cell being transmitted from a Master unit (element 10 in fig1). Jensen discloses a slave unit (element 14 in fig 1) receiving the ATM cell (Col 2 lines 8-24). Jensen also discloses a bus for exchanging information between master and slave units (element 12 in fig 1).

Jensen discloses a FIFO buffer (element 22 in fig 1) for storing incoming cells (Col 2 lines25-34).

Jensen discloses an address translation (calculation) unit (element 20 in fig 1).

Jensen discloses the translation unit including an ATM content addressable memory and look up table (register) as disclosed in Col 2 lines 36-45. Jensen discloses the translation unit accessing this memory and lookup table in order to generate the destination address within the slave (Col 2 lines 8-34).

Claim 2 Jensen discloses a FIFO buffer (element 22 in fig 1) for storing incoming cells (Col 2 lines25-34).

Claim 3, 16 Jensen discloses a FIFO unit capable of holding two cells (Col 2 lines 25-34).

Claim 7 Jensen discloses a slave unit containing a processor (element 18 in fig 1).

Claim 8 Jensen discloses data being passed to a UTOPIA bus (Col 5 lines 28-35).

Claim 14 Jensen discloses a master processing unit (fig 1 element10).

Jensen discloses a slave processing unit (Fig 1 element 14)

Jensen discloses a bus interfacing a master and slave, where the bus exchanges data between a master and slave (element 12 in fig 1).

The bus is connected to the slave, which consists of a FIFO buffer (element 22 in fig 1) for storing data (Col 2 lines25-34).

Jensen also discloses a an ATM content addressable memory as disclosed in Col 2 lines 36-45

Jensen discloses an address translation (calculation) unit (element 20 in fig 1).

Jensen discloses the address translation unit containing a memory, and the address translation unit connected to the FIFO buffer (Col 2 lines 36-45 and see fig 1)

Jensen discloses a look up table (register) within the address translation unit (Col 2 lines 36-45), where the address translation unit seeks a destination address, and routes data to the address port (Col 2 lines 25-35).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jensen et al. (US 6732206) in view of Thomas et al. (US 5941952)

Claim 4, 17 Jensen discloses a clock domain (Col 2 lines 46-65). However Jensen does not disclose the buffer storage unit transferring a data cell to the slave data processing unit every clock cycle.

Thomas et al ('Thomas' hereinafter) discloses circuitry for transmitting data from a buffer unit to an interface at a particular rate (Col2 lines 36-54).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify that master unit as disclosed by Jensen, to include Thomas' circuitry for controlling the data transfer rate to an interface, where the rate may be manipulated based on a user preference, so as to fulfill transferring of data every clock cycle. The motivation for the modification is to transfer data in a timely manner so as to prevent delays (Col 1 lines7-11 and Col 2 lines 6-35).

5. Claims 5, 6, 9, 10, 12, 13, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jensen et al. (US 6732206) in view of Kessler et al. (6029212).

Claim 5 Jensen discloses using an address translation unit to determine a destination (Col 2 lines 8-24). However, Jensen does not disclose the destination locations being selected from a group of a plurality of central processing units and memory locations, at least one central processing unit and at least one memory location.

Kessler et al. ('Kessler' hereinafter) discloses a translation unit for calculating an address of a memory location, and transferring the data to one (selected) of a multiple number of external registers (Col 2 lines 5-17).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to specify the result of the translation (destination) as disclosed by Jensen, to include external registers, where registers are memory oriented and have several processing functions. The motivation for this specification is to address data to a specific location (Col1 lines12-15).

Claim 6 Jensen discloses a FIFO buffer (element 22 in fig 1) for storing data cells (Col 2 lines25-34). Jensen also discloses the FIFO being connected to a processor (elements 22 and 18 in fig 1).

Jensen discloses the FIFO buffer connected to a data bus, furthermore connected to a master, where the bus transports data.

Jensen does not specifically disclose the output unit exchanging information with the master processing unit. However Kessler discloses an I/O

controller for receiving and sending messages to a master, where the controller also includes buffering for the input and output data (Col 20 lines 40-52).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the slave unit as disclosed by Jensen to include the controller as disclosed by Kessler for allowing the capability to receive and transmit data to another unit.

Claim 9 Jensen does not disclose the slave processing unit including a direct memory access unit.

Kessler discloses the slave unit coupled to a direct memory access unit that transmits requests (Col 20 lines 40-52).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the slave unit as disclosed by Jensen to include a direct memory access unit as disclosed by Kessler. The motivation for this combination is to allow easier and direct access to memory.

Claim 10 Jensen discloses a FIFO buffer (element 22 in fig 1) for storing cells incoming from a master unit (Col 2 lines25-34 and see fig 1 elements 10 and 22).

Jensen discloses the translation unit including an ATM content addressable memory and look up table (register) as disclosed in Col 2 lines 36-45.

Jensen discloses the translation unit accessing this memory and lookup table in order to generate the destination address within the slave (Col 2 lines 8-34).

Jensen discloses after address translation, routing the data from the FIFO to their respective destinations (Col 2 lines 25-35). However, Jensen does not specifically disclose transmitting when storage space is available.

Kessler discloses after performing address translation, transferring data from memory (buffer) to an addressed external register (Col 2 lines 5-17). Furthermore, Kessler discloses each register maintaining a status of FULL or EMPTY where appropriate (Col 6 lines 9-19).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the slave processor as disclosed by Jensen, to inquire about a state of availability as disclosed by Kessler. The motivation for this combination is to avoid failure of delivery due to congestion and delay (Col 6 lines 9-19).

Claim 12 Jensen discloses data being passed to a UTOPIA bus (Col 5 lines 28-35).

Claim 13, 15 Jensen does not disclose the processing unit including a direct memory access unit, and applying the signal identifying the destination location to the direct memory access unit.

Kessler discloses the slave unit coupled to a direct memory access unit that transmits requests and is coupled to a slave unit (Col 20 lines 40-52).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the slave unit as disclosed by Jensen to include a direct memory access unit as disclosed by Kessler, where a request may be

dedicated for retrieving a destination address. The motivation for this combination is to allow easier and direct access to memory.

6. Claims 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jensen et al. (US 6732206) in view of Kessler et al. (6029212) in further view of Thomas et al. (US 5941952) .

Claim 11 Jensen discloses a FIFO unit capable of holding two cells (Col 2 lines 25-34).

The combined teachings of Jensen and Kessler do not specifically transferring a data cell from the buffer storage unit to the ATM slave processing unit on consecutive cycles

Thomas et al ('Thomas' hereinafter) discloses circuitry for transmitting data from a buffer unit to an interface at a particular rate (Col2 lines 36-54).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the combined teachings of Jensen and Kessler, to include Thomas' circuitry for controlling the data transfer rate to an interface, where the rate may be manipulated based on a user preference, so as to fulfill transferring of data every clock cycle. The motivation for the modification is to transfer data in a timely manner so as to prevent delays (Col 1 lines7-11 and Col 2 lines 6-35).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

(a) Wing So (US 6141744) discloses an interface device between a master and slave device containing a FIFO buffer, a register and digital signal processors.

(b) Watkins (US 5983332) discloses an apparatus and method for translating an address, containing FIFO buffers, memory, address translation unit and processors.

(c) Bowes et al. (US 5805927) discloses a direct memory access controller connected to the CPU bus of a computer system (slave unit). Bowes also discloses a number of registers.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher P Grey whose telephone number is (571)272-3160. The examiner can normally be reached on 6:30-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (571)272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher Grey
Examiner
Art Unit 2667

5/4/05

AFSAR QURESHI
PRIMARY EXAMINER

5/9/05